Claims

[c1] An electronic automation system comprising:
a shape-based database of an integrated circuit design;
a mouse input device;
a graphical user interface tool, capable of accessing and performing operations on the shape-based database, based on input from the mouse input device; and
an automatic router tool, capable of accessing the shape-based database, to create a interconnect route path for at least one net of the integrated circuit design, selected using the graphical user interface tool and the mouse, wherein the interconnect route path comprises segments having different interconnect widths.

[c2] The system of claim 1 further comprising:
a file, accessible by the automatic router tool, comprising a current density table comprising current density as a function of at least one of layer, net frequency, or track width, accessible by the automatic router tool.

[c3] The system of claim 1 further comprising:
a file, accessible by the automatic router tool, comprising frequency information for one or more nets of integrated circuit, wherein when frequency information is

not provided for a net, DC operation of the net will be assumed.

[c4] The system of claim 1 further comprising:
a file, accessible by the automatic router tool, comprising frequency information for one or more nets of integrated circuit, wherein when frequency information is not provided for a net, a warning message is presented.

[c5] The system of claim 1 wherein the automatic router tool uses at least one of Steiner tree algorithm, heuristic Steiner tree creation algorithm, or Batched Greedy Algorithm.

[c6] The system of claim 1 further comprising:
a data import interface tool, wherein the data input interface tool takes a file having an integrated circuit design created on another electronic design automation system and generates a shape-based database of the integrated circuit design, which will be accessible and operated on by the electronic automation system.

[c7] The system of claim 1 wherein the integrated circuit design comprises at least one of a memory integrated circuit, DRAM, EPROM, EEPROM, Flash memory, ASIC, microprocessor, programmable logic device, field programmable gate array, digital signal processor, analog

integrated circuit, amplifier circuit, system on a chip, or programmable system-on-a-chip.

[c8] The system of claim 1 wherein automatic router tools creates interconnect route paths for two or more nets, and the interconnect route paths are for one layer of the integrated circuit design.

[c9] A method of designing an integrated circuit comprising:
determining an interconnect route path between a first point and a second point of an integrated circuit design;
comparing a property of the interconnect route path to a design rule;
if the property of the first interconnect path violates the design rule, creating an interconnect line for the interconnect route path having a first width; and
if the property of the first interconnect path meets the design rule, creating the interconnect line for the interconnect route path having a second width, different from the first width.

[c10] The method of claim 9 wherein the property is a current requirement of the interconnect route path.

[c11] The method of claim 9 wherein the design rule is a current density rule.

[c12] The method of claim 9 wherein the design rule is an op-

tical proximity effect correction rule.

[c13] A method of designing an integrated circuit comprising:
determining an interconnect route path between a first point and a second point of an integrated circuit design;
determining a property of the interconnect route path; and
creating an interconnect line for the interconnect route path having a width based on the property of the interconnect route path and a design rule.

[c14] The method of claim 13 wherein the design rule addresses at least one of current density, optical proximity effects, current handling, power handling, reliability, electromigration, voltage drop, or self-heating.

[c15] The method of claim 13 wherein the determining an interconnect route path between a first point and a second point of an integrated circuit design uses a gridless approach.

[c16] The method of claim 13 wherein the determining an interconnect route path between a first point and a second point of an integrated circuit design uses a shape-based approach.

[c17] The method of claim 13 wherein the determining an interconnect route path between a first point and a second

point of an integrated circuit design uses a gridded approach.

[c18] A computer program product stored on a computer-readable storage medium for designing an integrated circuit, the computer program product comprising:
code for determining an interconnect route path between a first point and a second point of an integrated circuit design;
code for determining a property of the interconnect route path; and
code for creating an interconnect line for the interconnect route path having a width based on the property of the interconnect route path and a design rule.

[c19] The computer program product of claim 18 wherein the design rule addresses at least one of current density, optical proximity effects, current handling, power handling, reliability, electromigration, voltage drop, or self-heating.

[c20] The computer program product of claim 18 wherein the determining an interconnect route path between a first point and a second point of an integrated circuit design uses a shape-based approach.